IN THE SPECIFICATION:

Please insert the following new paragraph at page 1, line 1 of specification:

This application is a continuation of Application Serial No. 09/652,984, filed August 31, 2000.

Kindly replace the thirteen paragraphs starting at page 1, line 10 and continuing to page 2, line 17 with the following:

U.S. Patent Application Ser. No. 09/652,644 ~~(15311-2281)~~ entitled ADAPTIVE DATA PREFETCH PREDICTION ALGORITHM;

U.S. Patent Application Ser. No. 09/653,133 ~~(15311-2282)~~ entitled UNIQUE METHOD OF REDUCING LOSSES IN CIRCUITS USING V^2 PWM CONTROL;

U.S. Patent Application Ser. No. 09/652,641 ~~(15311-2283)~~ entitled IO SPEED AND LENGTH PROGRAMMABLE WITH BUS POPULATION;

U.S. Patent Application Ser. No. 09/652,458 ~~(15311-2284)~~ entitled PARTITION FORMATION USING MICROPROCESSORS IN A MULTIPROCESSOR COMPUTER SYSTEM;

U.S. Provisional Patent Application Ser. No. 60/304,167 ~~(15311-2285)~~ entitled SYSTEM AND METHOD FOR USING FUNCTION NUMBERS TO INCREASE THE COUNT OF OUTSTANDING SPLIT TRANSACTIONS;

U.S. Patent Application Ser. No. 09/653,180 ~~(15311-2287)~~ entitled ONLINE ADD/REMOVAL OF SERVER MANAGEMENT INFRASTRUCTURE;

U.S. Patent Application Ser. No. 09/652,494 ~~(15311-2288)~~ entitled AUTOMATED BACKPLANE CABLE CONNECTION IDENTIFICATION SYSTEM AND METHOD;

U.S. Patent Application Ser. No. 09/652,459 ~~(15311-2289)~~ entitled CLOCK FORWARDING DATA RECOVERY ~~AUTOMATED BACKPLANE CABLE CONNECTION IDENTIFICATION SYSTEM AND METHOD~~;

U.S. Patent Application Ser. No. 09/652,980 ~~(15311-2290)~~ entitled CLOCK FORWARD INITIALIZATION AND RESET SIGNALING TECHNIQUE;

U.S. Patent Application Ser. No. 09/944,515 ~~(15311-2292)~~ entitled PASSIVE RELEASE AVOIDANCE TECHNIQUE;

U.S. Patent Application Ser. No. 09/652,985 ~~(15311-2293)~~ entitled COHERENT TRANSLATION LOOK-ASIDE BUFFER;

U.S. Patent Application Ser. No. 09/652,645 ~~(15311-2294)~~ entitled DETERMINISTIC HARDWARE BEHAVIOR BETWEEN MULTIPLE ASYNCHRONOUS CLOCK DOMAINS THROUGH THE NOVEL USE OF A PLL; and

U.S. Patent Application Ser. No. 09/655,171 ~~(15311-2306)~~ entitled VIRTUAL TIME OF YEAR CLOCK.

Kindly replace the carryover paragraph between pages 5-6 with the following:

To prevent two I/O devices from becoming "livelocked" in response to competing requests for the same data, each I/O bridge further includes at least one non-coherent memory device which is also coupled to and thus under the control of the down engine. Before invalidating data requested by a competing ~~competed~~ device or entity, the down engine at the I/O bridge receiving the request first copies that data to the bridge's non-

coherent memory device. The down engine then takes the largest amount of the copied data that it "knows" to be coherent (despite the request for that data by a processor or other I/O bridge) and releases only that amount to the I/O device which originally requested the data from the bridge. In the illustrative embodiment, this "known" coherent amount of data corresponds to one I/O bus cycle. The remaining data that was copied into the non-coherent memory device is then discarded. In this way, the I/O device that originally requested the data is guaranteed to make at least some forward progress despite data collisions, and yet data coherency is still maintained within the I/O domain of the SMP computer system.